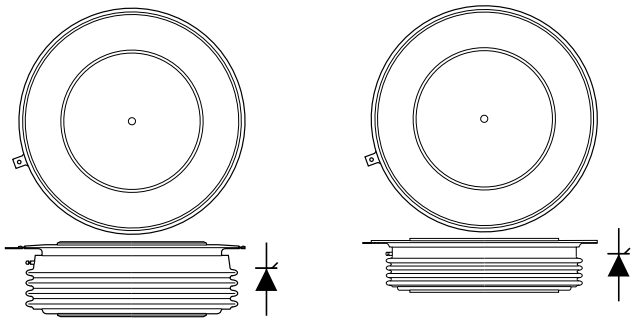
DCR1474SY / DCR1474SV

Phase Control Thyristor

Replaces July 2001 version, DS4649-6.0

DS4649-7.3 November 2002

PACKAGE OUTLINE



Outline type code: Y **Outline type code: V**

See Package Details for further information.

Fig. 1 Package outline

KEY PARAMETERS

V_{DRM}	**1800V**
$I_{T(AV)}$	**3600A**
I_{TSM}	**61200A**
dVdt*	**1000V/μs**
dI/dt	**300A/μs**

***Higher dV/dt selections available**

VOLTAGE RATINGS

Part Number	Repetitive Peak Voltages V_{DRM} V_{RRM} V	Conditions
DCR1474SY18 or DCR1474SV18	1800 1800	T_{vj} = 0˚ to 125˚C. I_{DRM} = I_{RRM} = 250mA. V_{DRM}, V_{RRM} = 10ms 1/2 sine. V_{DSM} & V_{RSM} = V_{DRM} & V_{RRM} + 100V respectively.

Lower voltage grades available.

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR1474SY18 for an 1800V 'Y' outline variant

or

DCR1474SV18 for an 1800V 'V' outline variant

If a lower voltage grade is required, then use V_{DRM}/100 for the grade required e.g.:

DCR1474SY16 for a 1600V 'Y' outline variant etc.

Note: Please use the complete part number when ordering and quote this number in any future correspondance relating to your order.

CURRENT RATING

T_{case} = 60˚C unless stated otherwise.

Symbol	Parameter	Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	3600	A
$I_{T(RMS)}$	RMS value	-	5655	A
I_T	Continuous (direct) on-state current	-	4996	A
Single Side Cooled (Anode side)				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	2279	A
$I_{T(RMS)}$	RMS value	-	3580	A
I_T	Continuous (direct) on-state current	-	2897	A

CURRENT RATING

T_{case} = 80˚C unless stated otherwise.

Symbol	Parameter	Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	2785	A
$I_{T(RMS)}$	RMS value	-	4370	A
I_T	Continuous (direct) on-state current	-	3750	A
Single Side Cooled (Anode side)				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	1750	A
$I_{T(RMS)}$	RMS value	-	2745	A
I_T	Continuous (direct) on-state current	-	2170	A

SURGE RATINGS

Symbol	Parameter	Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine; T_{case} = 125°C	49.0	kA
I^2t	I^2t for fusing	V_R = 50% V_{RRM} - 1/4 sine	12.0 x 10^6	A^2s
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine; T_{case} = 125°C	61.2	kA
I^2t	I^2t for fusing	V_R = 0	18.75 x 10^6	A^2s

THERMAL AND MECHANICAL DATA

Symbol	Parameter	Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	dc	-	0.0095	°C/W
		Single side cooled	Anode dc	-	0.019	°C/W
			Cathode dc	-	0.019	°C/W
$R_{th(c-h)}$	Thermal resistance - case to heatsink	Clamping force 43kN with mounting compound	Double side	-	0.002	°C/W
			Single side	-	0.004	°C/W
T_{vj}	Virtual junction temperature	On-state (conducting)		-	135	°C
		Reverse (blocking)		-	125	°C
T_{stg}	Storage temperature range			–55	125	°C
-	Clamping force			38	47	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Conditions		Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM}, T_{case} = 125°C		250	mA
dV/dt	Maximum linear rate of rise of off-state voltage	To 67% V_{DRM} T_j = 125°C.		1000	V/µs
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to 1000A Gate source 20V, 10Ω $t_r \leq 0.5$µs to 1A, T_j = 125°C	Repetitive 50Hz	150	A/µs
			Non-repetitive	300	A/µs
$V_{T(TO)}$	Threshold voltage	At T_{vj} = 125°C		0.92	V
r_T	On-state slope resistance	At T_{vj} = 125°C		0.09	mΩ
t_{gd}	Delay time	V_D = 67% V_{DRM}, Gate source 30V, 15Ω $t_r \leq 0.5$µs, T_j = 25°C		2	µs
t_q	Turn-off time	I_T = 1000A, t_p = 1ms, T_j = 125˚C, V_R = 50V, dI_{RR}/dt = 20A/µs, V_{DR} = 67% V_{DRM}, dV_{DR}/dt = 20V/µs linear		200	µs
I_L	Latching current	T_j = 25°C, V_D = 5V		1000	mA
I_H	Holding current	T_j = 25°C, R_{g-k} = ∞		300	mA

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V_{DRM} = 5V, T_{case} = 25°C	4.0	V
I_{GT}	Gate trigger current	V_{DRM} = 5V, T_{case} = 25°C	400	mA
V_{GD}	Gate non-trigger voltage	At V_{DRM} T_{case} = 125°C	0.25	V
V_{FGM}	Peak forward gate voltage	Anode positive with respect to cathode	30	V
V_{FGN}	Peak forward gate voltage	Anode negative with respect to cathode	0.25	V
V_{RGM}	Peak reverse gate voltage		5	V
I_{FGM}	Peak forward gate current	Anode positive with respect to cathode	30	A
P_{GM}	Peak gate power	See table, gate characteristics curve	150	W
$P_{G(AV)}$	Mean gate power		10	W

CURVES

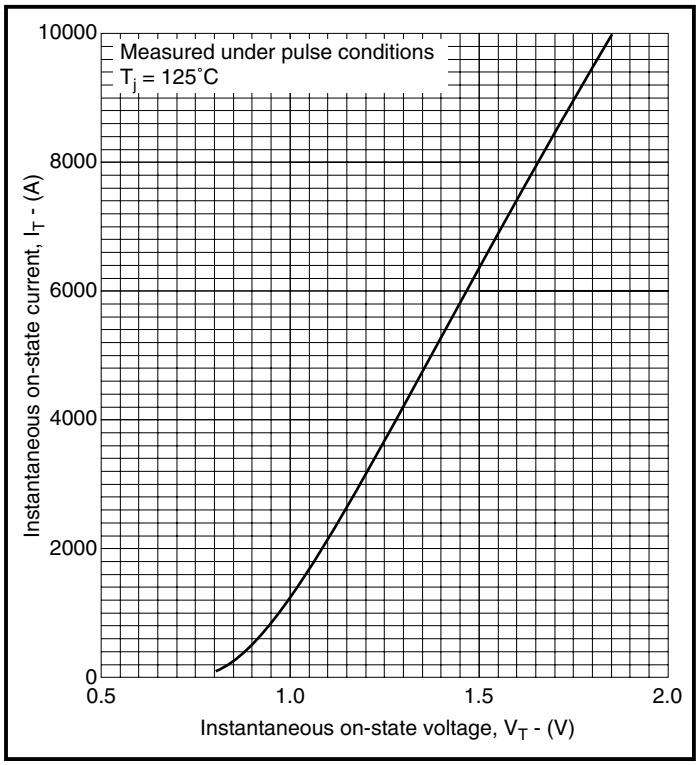


Fig.2 Maximum (limit) on-state characteristics

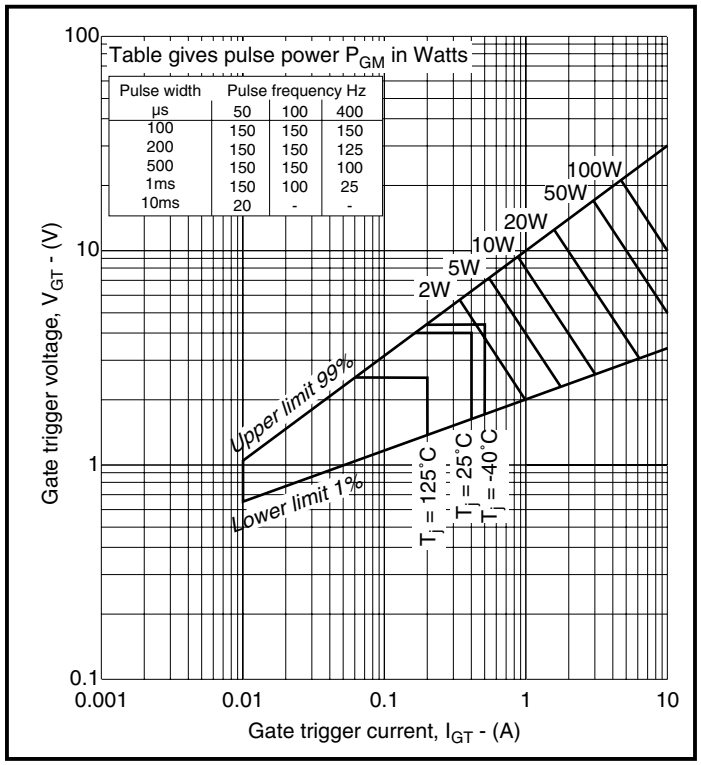


Fig.3 Gate characteristics

V_{TM} Equation:-

$$V_{TM} = A + B\ln(I_T) + C.I_T + D.\sqrt{I_T}$$

Where A = 0.7635305
B = 8.73036 x 10^{-3}
C = 8.568357 x 10^{-5}
D = 1.537158 x 10^{-3}

These values are valid for T_j = 125˚C for I_T 500A to 10000A

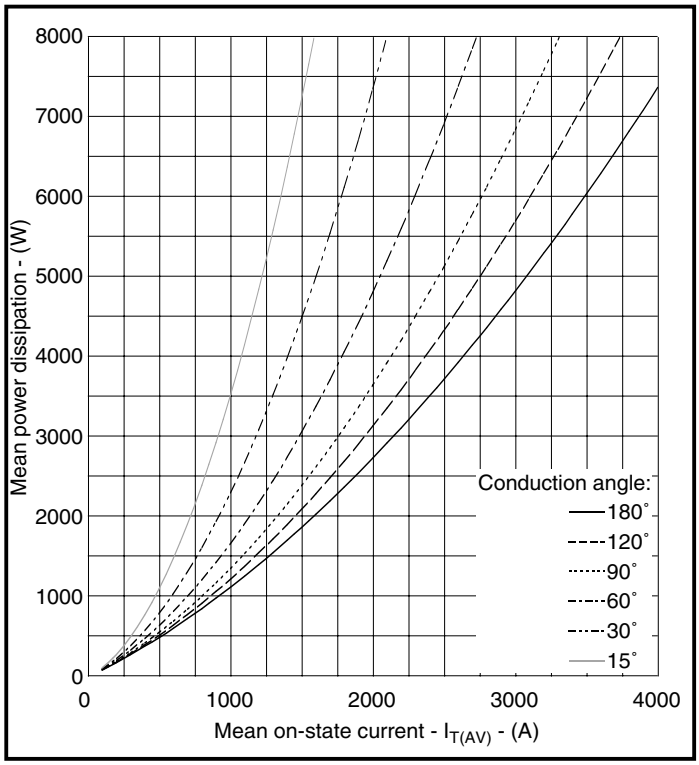


Fig.4 Dissipation curves - sine wave

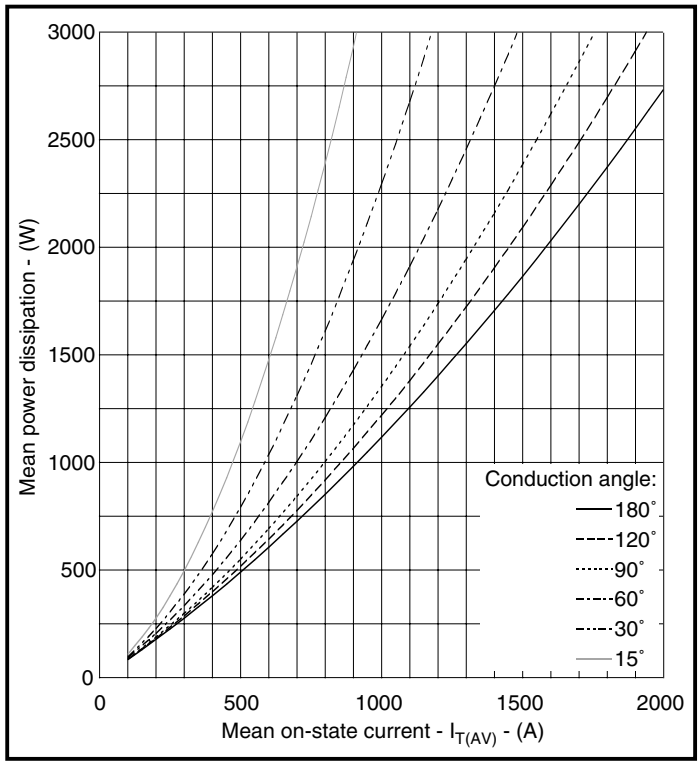


Fig.5 Dissipation curves - sine wave

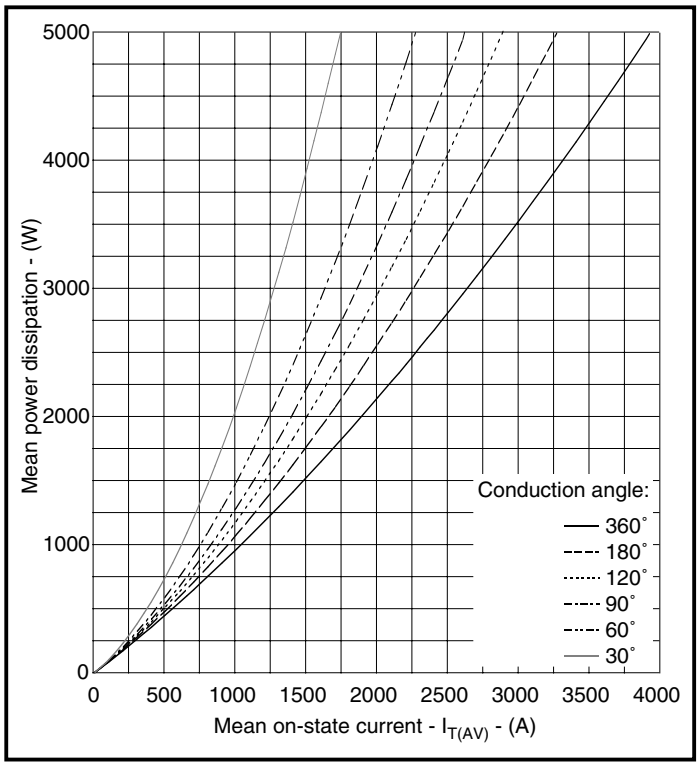


Fig.6 Dissipation curves - square wave

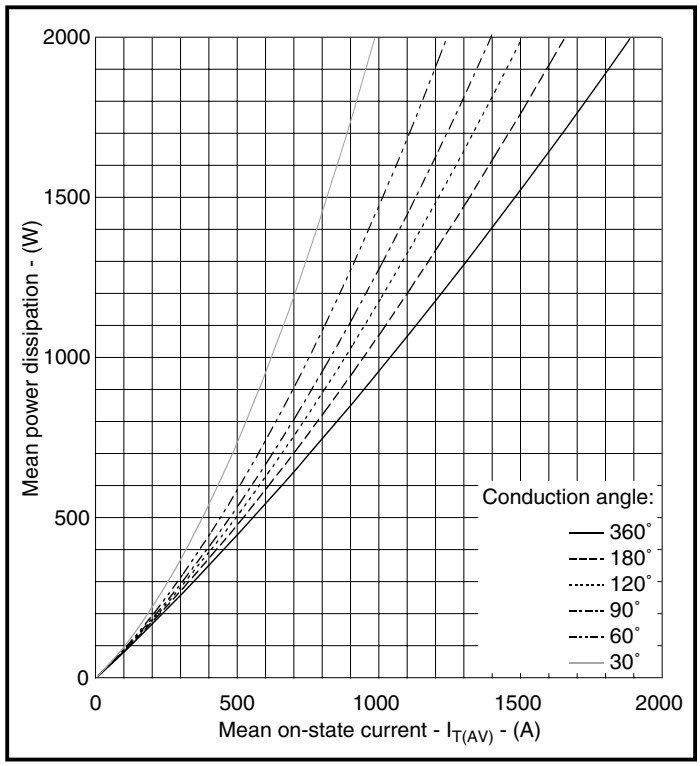


Fig.7 Dissipation curves - square wave

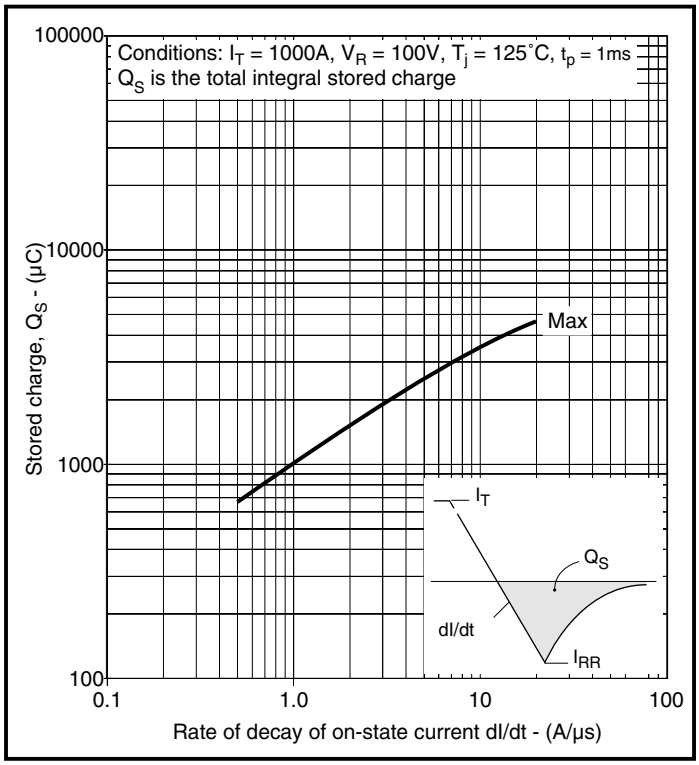


Fig.8 Stored charge

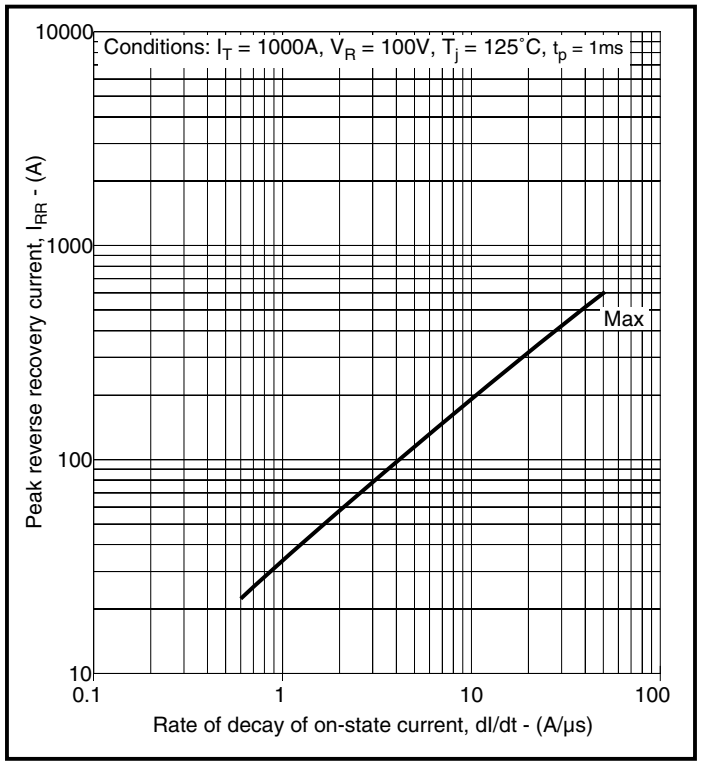
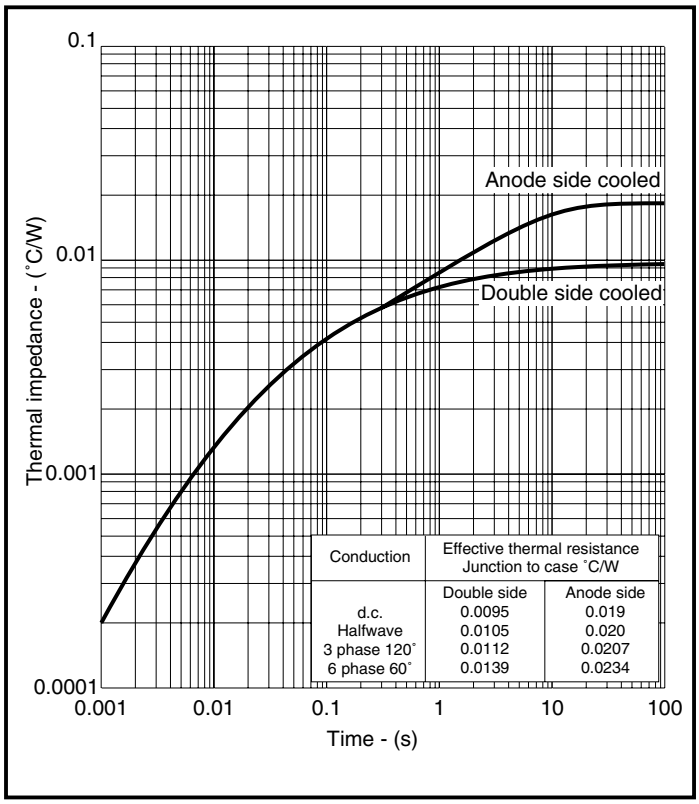


Fig.9 Reverse recovery current



Conduction	Effective thermal resistance Junction to case ˚C/W	
	Double side	Anode side
d.c.	0.0095	0.019
Halfwave	0.0105	0.020
3 phase 120˚	0.0112	0.0207
6 phase 60˚	0.0139	0.0234

Fig.10 Transient thermal impedance - junction to case

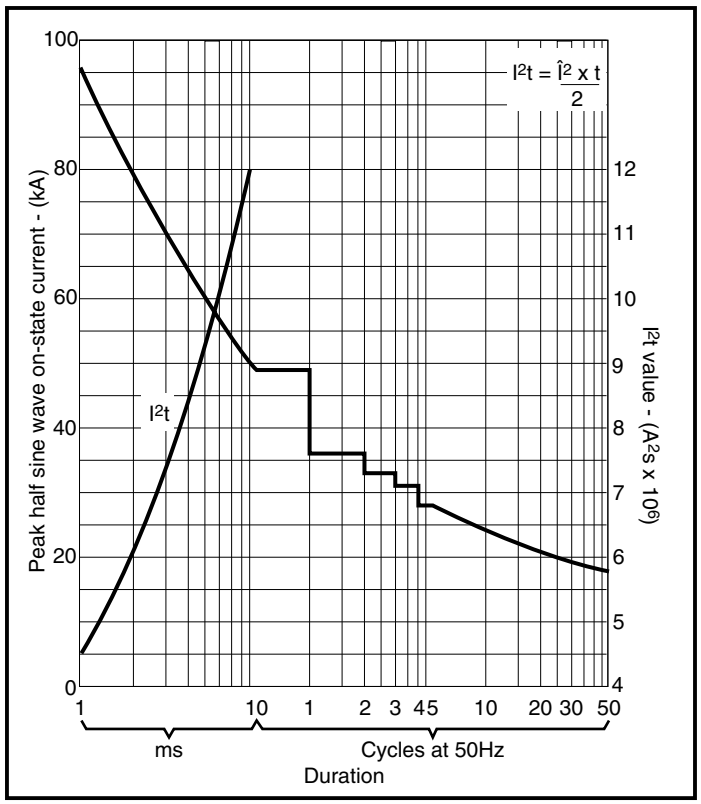
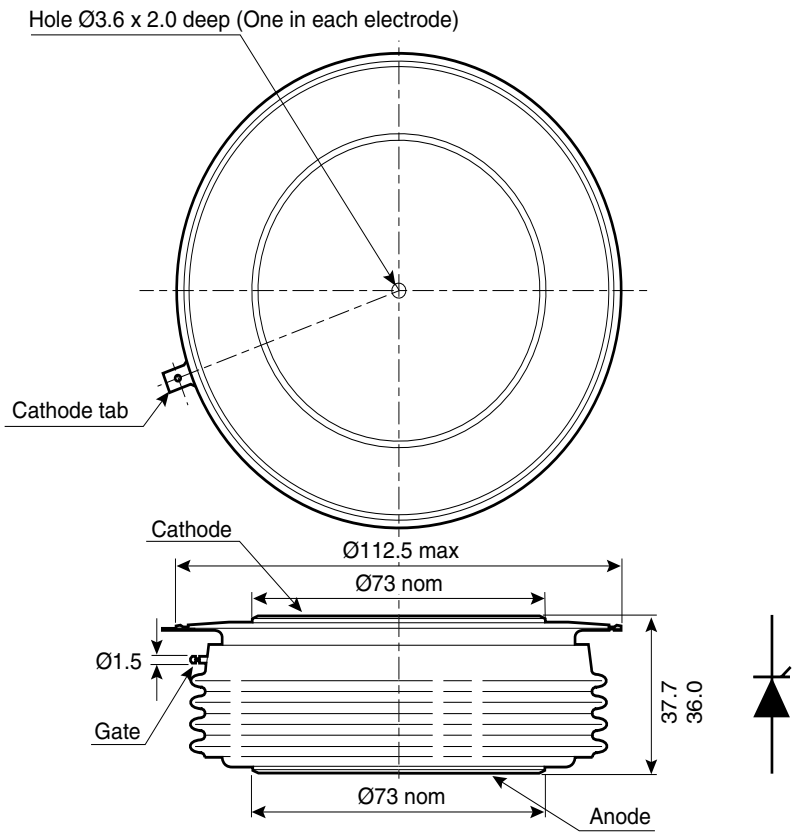


Fig.11 Surge (non-repetitive) on-state current vs time (with 50% V_{RRM} at T_{case} = 125˚C)

PACKAGE DETAILS

For further package information, please contact Customer Service. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



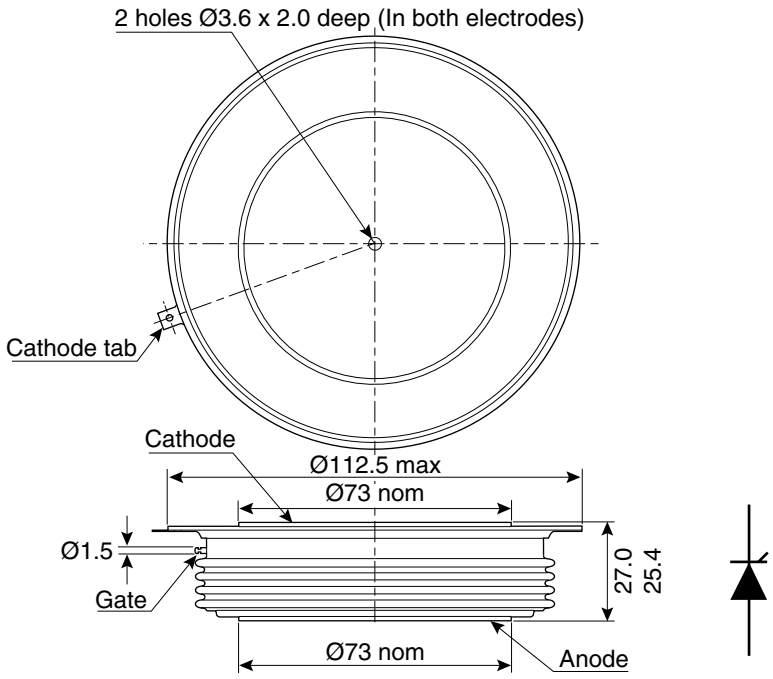
Nominal weight: 1600g
Clamping force: 43kN ±10%

Package outline type code: Y

Fig.12 Package details

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



Nominal weight: 1100g
Clamping force: 43kN ±10%
Lead length: 420mm
Lead terminal connector: M4 ring

Package outline type code: V

Fig.13 Package details

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.

http://www.dynexsemi.com

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