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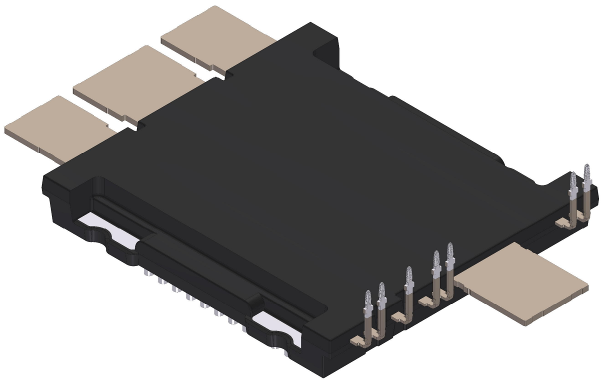
Data sheet 5SYA 629238 Preliminary

5SFG 0780B120000

RoadPak SiC phase leg module 1200 V, 780 A*

- V_{DSS} = 1200 V
- I_D = 2 x 780 A*
- Molded package optimized for e-Mobility application
- Pin-fin structure for lowest thermal resistance
- Lowest losses thanks to Silicon Carbide chip set
- Main terminals with holes for screw connection or without holes for welding



*Current rating based on chip rating times number of chips

Maximum rated values [1)]

Parameter	Symbol	Conditions	Min.	Max.	Unit
Drain-source voltage	V_{DS}	V_{GS} = 0 V, T_{vj} ≥ -40 °C		1200	V
DC drain current	I_D	T_{Cool} = 55 °C, T_{vj} = 175 °C		540	A
Peak drain current	I_{DM}	t_p = 1 ms, limited by T_{jmax}		1200	A
Recommended static gate - source voltage	$V_{GS,DC}$		-4	15	V
Max gate - source voltage [2)]	$V_{GS,max, DC}$		-8	16	V
DC reverse drain current (body diode)	I_{DR}	V_{GS} = -4 V, T_{Cool} = 55 °C, T_{vj} = 175 °C		330	A
Peak reverse drain current (body diode)	I_{DRM}	V_{GS} = -4 V, t_p = 1 ms		1200	A
Surge source current (body diode)	I_{SSM}	V_{GS} = -4 V, T_{vj} = 175 °C, t_p = 10 ms, half-sinewave		2500	A
DC reverse drain current (channel open)	I_{DRS}	V_{GS} = 15 V, T_{Cool} = 55 °C, T_{vj} = 175 °C		540	A
Surge source current (channel open)	I_{SSX}	V_{GS} = 15 V, T_{vj} = 175 °C, tp = 10 ms, half-sinewave		2500	A
MOSFET short circuit SOA	t_{psc}	V_{DD} = 850 V, V_{GS} = -4/15 V, T_{vj} ≤ 175 °C		1.2	µs
Isolation voltage	V_{isol}	1 min, f = 50 Hz		3300	V
Junction temperature	T_{vj}			175	°C
Junction operating temperature	$T_{vj(op)}$		-40	175	°C
Storage temperature	T_{stg}		-40	150	°C
Mounting torque	M_s	Module to cooler with M4 screws	2.6	3.1	Nm

[1)] Maximum rated values indicate limits beyond which damage to the device may occur per IEC 60747
[2)] Based on chip capability

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MOSFET characteristic values [3)]

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA	T_{vj} = 175 °C	1200			V
			T_{vj} = 25 °C	1200			V
			T_{vj} = -40 °C	1200			V
Static drain-source on-state resistance [4)]	$R_{DS(on)}$	I_D = 540 A, V_{GS} = 15 V	T_{vj} = 25 °C		2.2	2.5	mΩ
			T_{vj} = 175 °C		4.1	4.6	mΩ
Zero gate voltage drain current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V	T_{vj} = 25 °C		2	10	µA
			T_{vj} = 175 °C		5	20	µA
Gate-source leakage current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 15 V, T_{vj} = 25 °C				500	nA
Gate threshold voltage [2)]	$V_{GS(th)}$	I_D = 160 mA, V_{DS} = V_{GS}, T_{vj} = 25 °C		1.8	2.5	3.6	V
Gate charge [2)]	Q_G	I_D = 580 A, V_{DS} = 800 V, V_{GS} = -4 V ... +15 V			1.6		µC
Input capacitance [2)]	C_{ISS}	V_{DS} = 1000 V, V_{GS} = 0 V, T_{vj} = 25 °C, f = 100 kHz			50.4		nF
Internal gate resistance [2)]	R_{Gint}	f = 1 MHz, V_{AC} = 25 mV, per switch			0.43		Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 800 V, I_D = 600 A, R_G = 0.47 Ω, C_{GS} = 47 nF, V_{GS} = -4 / +15 V, L_σ = 10 nH, inductive load	T_{vj} = 25 °C		50		ns
			T_{vj} = 175 °C		50		ns
Rise time	t_r		T_{vj} = 25 °C		140		ns
			T_{vj} = 175 °C		120		ns
Turn-off delay time	$t_{d(off)}$	V_{DD} = 800 V, I_D = 600 A, R_G = 1 Ω, C_{GS} = 47 nF, V_{GS} = -4 / +15 V, L_σ = 10 nH, inductive load	T_{vj} = 25 °C		240		ns
			T_{vj} = 175 °C		260		ns
Fall time	t_f		T_{vj} = 25 °C		60		ns
			T_{vj} = 175 °C		60		ns
Turn-on switching energy	E_{on}	V_{DD} = 800 V, I_D = 600 A, R_G = 0.47 Ω, C_{GS} = 47 nF, V_{GS} = -4 / +15 V, L_σ = 10 nH, inductive load	T_{vj} = 25 °C		24		mJ
			T_{vj} = 175 °C		30		mJ
Turn-off switching energy	E_{off}	V_{DD} = 800 V, I_D = 600 A, R_G = 1 Ω, C_{GS} = 47 nF, V_{GS} = -4 / +15 V, L_σ = 10 nH, inductive load	T_{vj} = 25 °C		16		mJ
			T_{vj} = 175 °C		16		mJ
Short circuit current	I_{SC}	t_{on} ≤ 1.2 µs, V_{GS} = 15 V, V_{DD} = 850 V, $V_{DSM\ CHIP}$ ≤ 1200 V	T_{vj} = 175 °C		7800		A

[2)] Based on chip capability
[3)] Characteristic values according to IEC 60747 – 8
[4)] R_{DSon} is given at chip level

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Body diode characteristic values [5]

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Diode forward voltage [2) 6)]	V_{SD}	I_S = 290 A, V_{GS} = -4 V	T_{vj} = 25 °C		4.7		V
			T_{vj} = 175 °C		4.2		V
Reverse recovery current	I_{rr}	V_{DS} = 800 V, I_{SD} = 600 A, V_{GS} = -4 / +15 V, R_G = 0.47 Ω, C_{GS} = 47 nF, di/dt = 15 kA/µs, L_σ = 10 nH, inductive load	T_{vj} = 25 °C		140		A
			T_{vj} = 175 °C		380		A
Recovered charge	Q_{rr}		T_{vj} = 25 °C		10		µC
			T_{vj} = 175 °C		18		µC
Reverse recovery time	t_{rr}		T_{vj} = 25 °C		30		ns
			T_{vj} = 175 °C		50		ns
Reverse recovery energy	E_{rec}		T_{vj} = 25 °C		2		mJ
			T_{vj} = 175 °C		7		mJ

[2] Based on chip capability
[5] Characteristic values according to IEC 60747 – 2
[6] Forward voltage is given at chip level

Package properties [7]

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Thermal resistance [8] junction to fluid	$R_{th(j-f)}$	T_{in} = 65°C, Coolant: 50% glycol/ 50% water, per switch, 10 L/min, dp < 120 mbar			92	96.6	K/kW
Comparative tracking index	CTI			400			V
Module stray inductance	L_σ				5		nH
Resistance, terminal-chip	$R_{DD'+SS'}$		T_c = 25 °C		0.117		mΩ
			T_c = 150 °C		0.227		mΩ

[7] Package and mechanical properties according to IEC 60747 – 1
[8] See Fig. 16 .. 23 for more information

NTC Thermistor

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Rated resistance	R_{25}	T_c=25 °C		4700		Ω
R100	R_{100}	T_c=100 °C		457.9		Ω
B-value	$B_{25/85}$	$R = R_{25} \exp [B_{25/85}(1/T – 1/(298.15K))]$		3435		K

Mechanical properties [7]

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Dimensions	L	AC terminal to DC terminal			110		mm
	W	Mold width			69		mm
	H	Baseplate cooler surface to middle of PCB/pressfit			17.35		mm
Clearance distance in air	d_a	According to IEC 60664-1	Term. to Base:		6.9		mm
			Term. to Term.:		3.3		mm
Surface creepage distance	d_s	According to IEC 60664-1	Term. to Base:		8.5		mm
			Term. to Term.:		8		mm
Mass	m				310		g

[7] Package and mechanical properties according to IEC 60747 – 1

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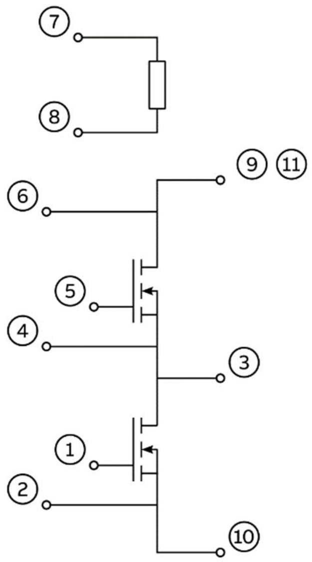
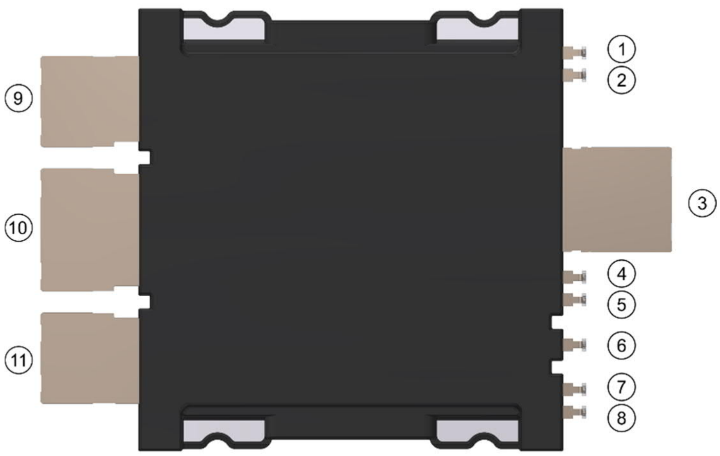
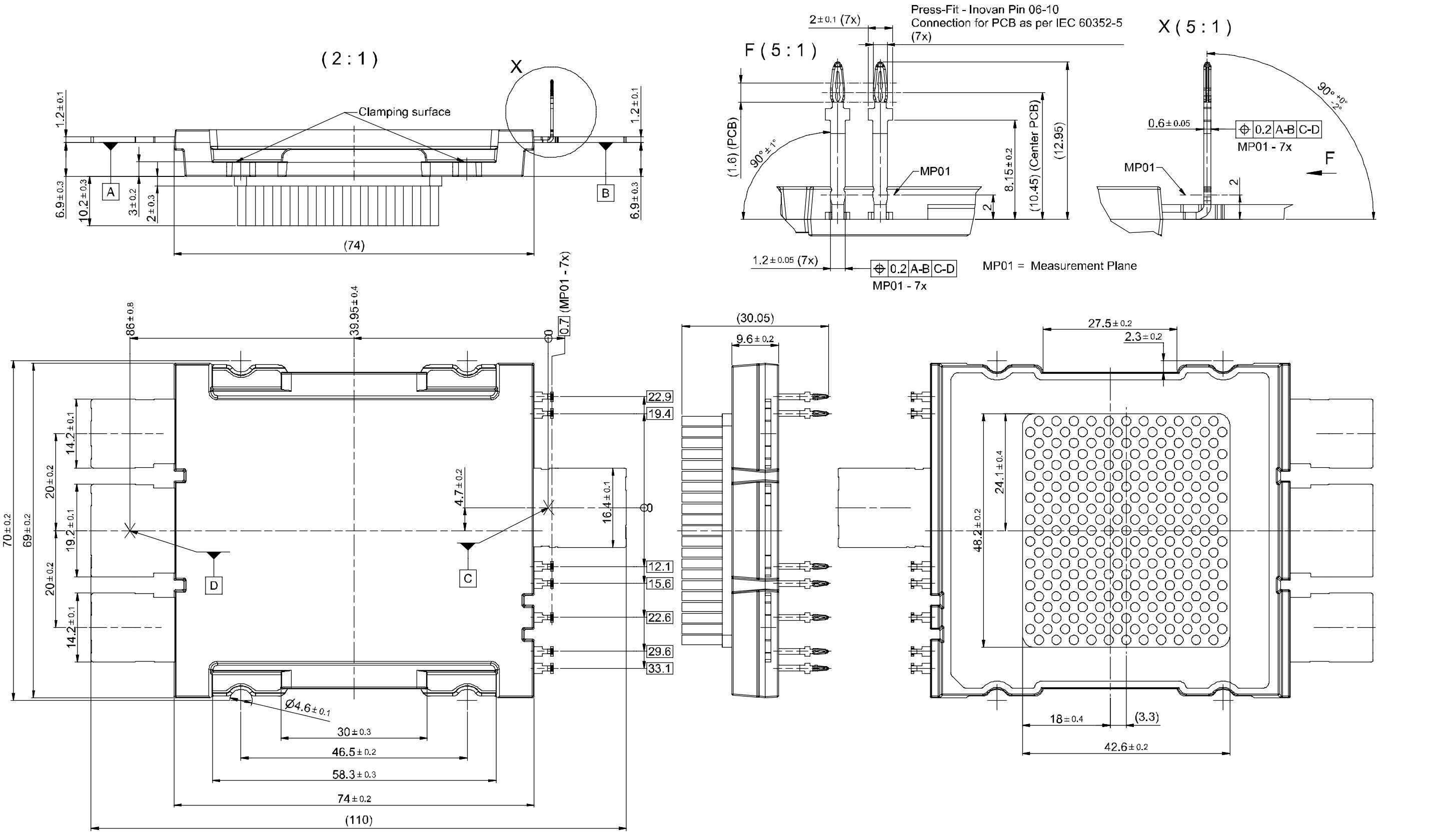
Electrical configuration



1 → Gate LS
2 → Source LS
3 → AC
4 → Source HS
5 → Gate HS
6 → Drain HS
7,8 → NTC
9 → DC+
10 → DC-
11 → DC+



Mechanical drawing



Note: all dimensions are shown in millimeters

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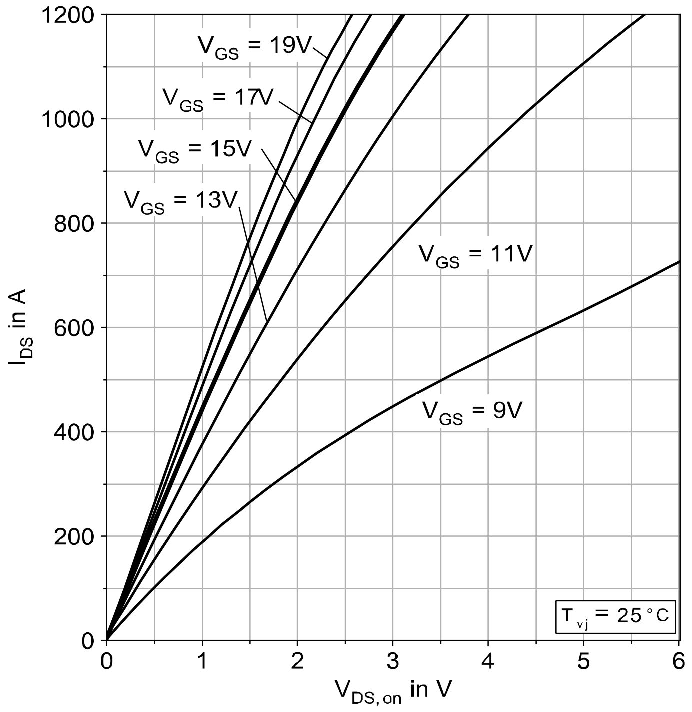

Fig. 1 Typical output characteristics

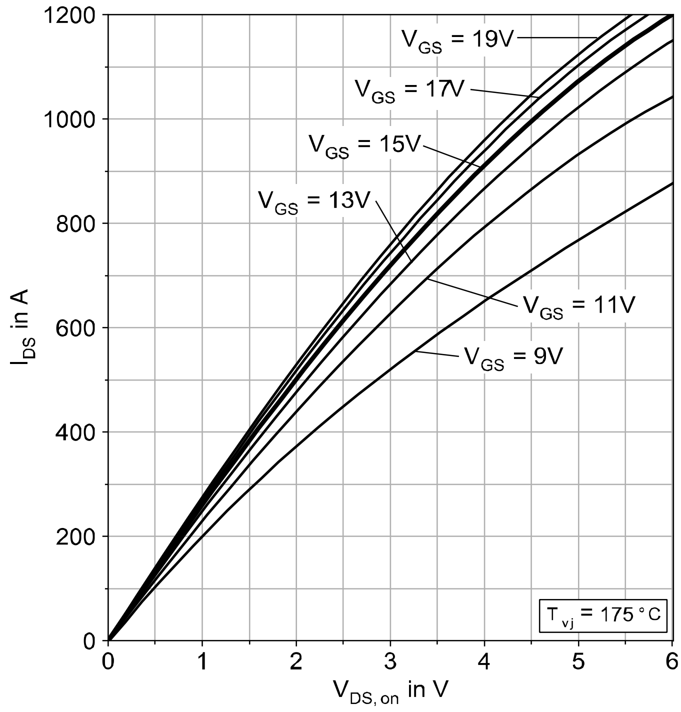

Fig. 2 Typical output characteristics

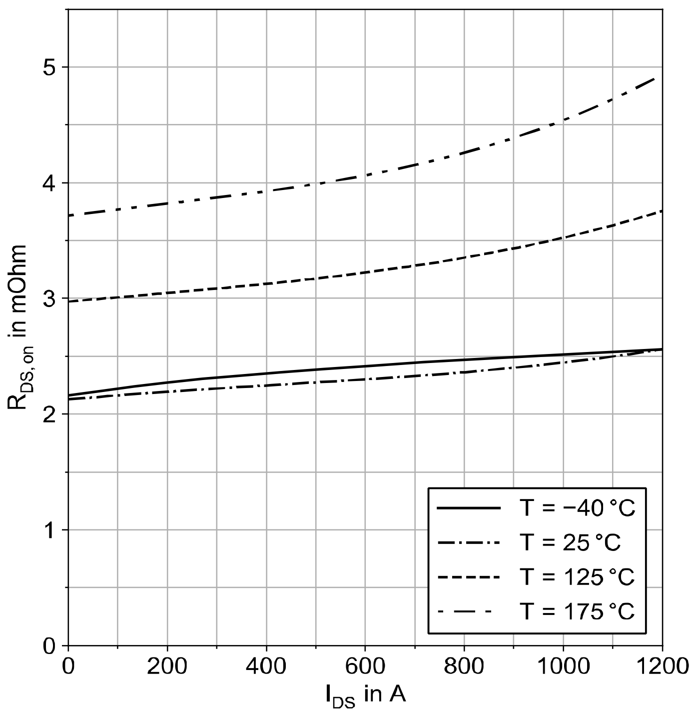

Fig. 3 Typical on-state resistance vs drain current for various junction temperatures

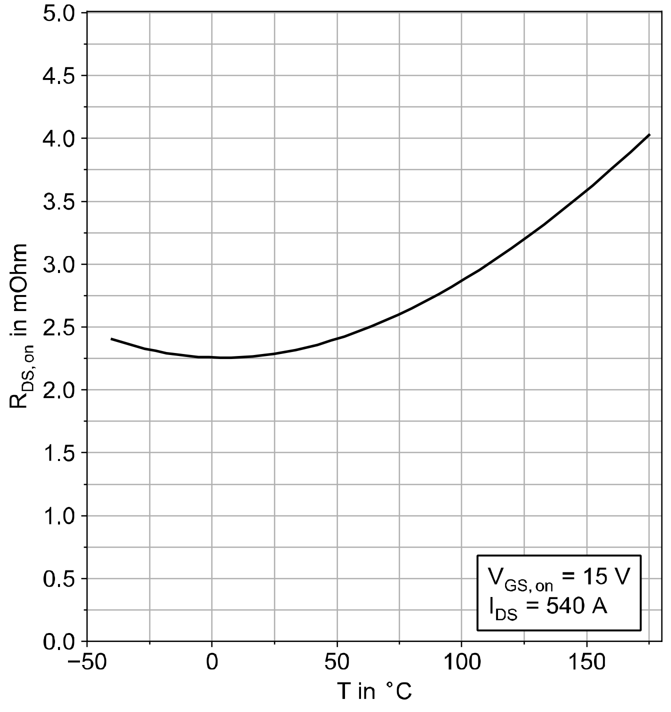

Fig. 4 Typical on-state resistance vs temperature

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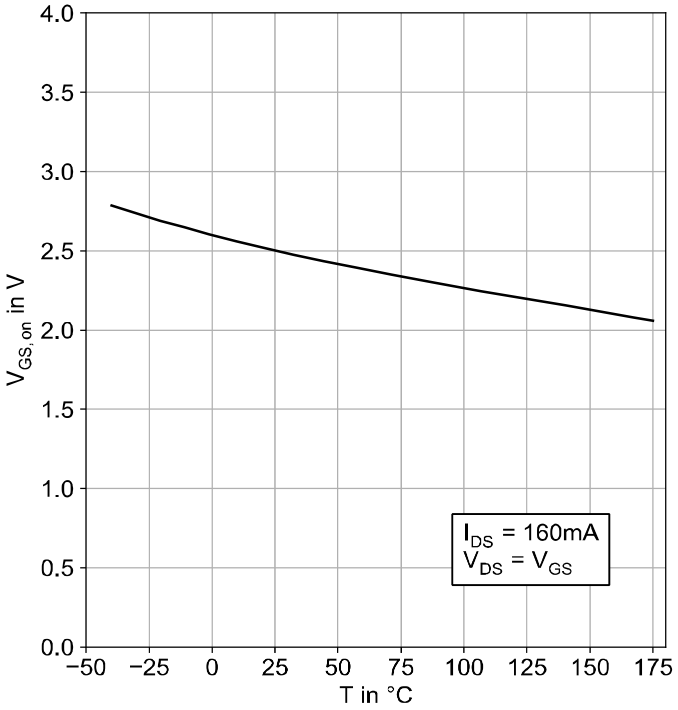

Fig. 5 Threshold voltage vs junction temperature

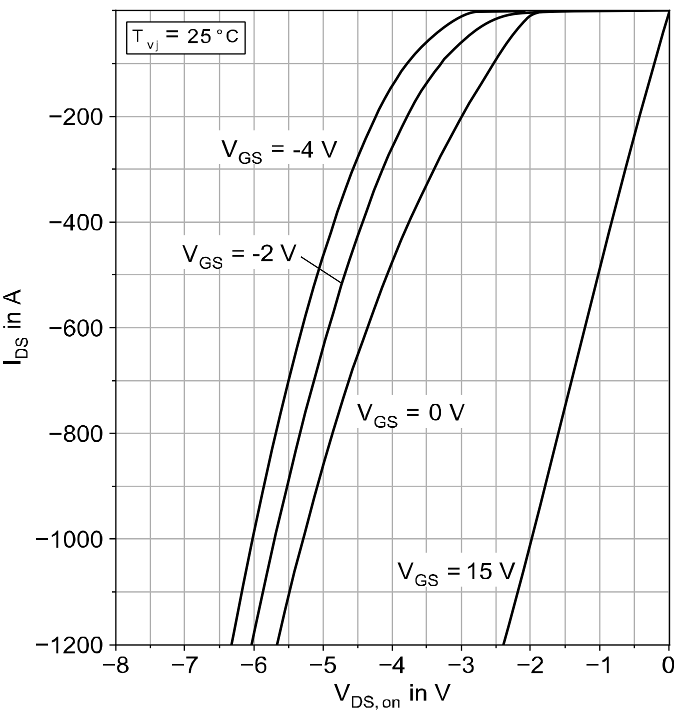

Fig. 6 Typical 3rd quadrant characteristics vs drain current

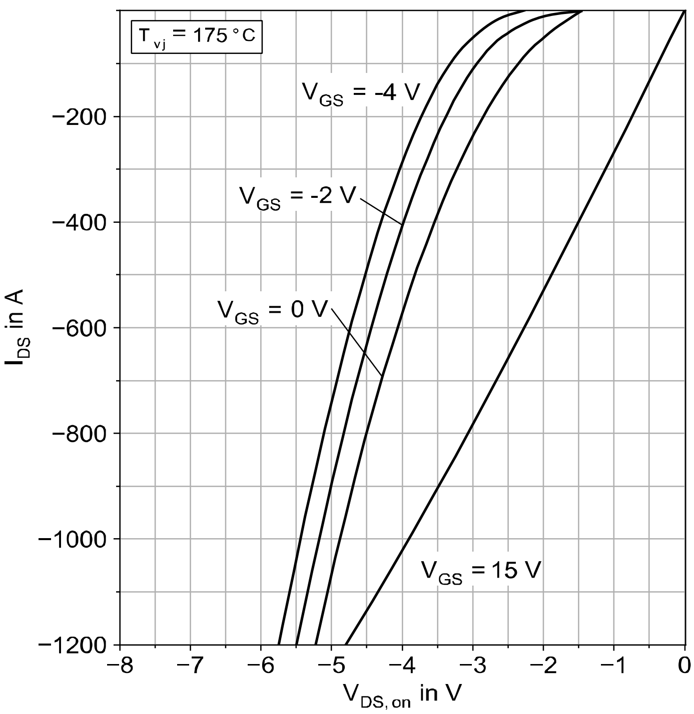

Fig. 7 Typical 3rd quadrant characteristics vs drain current

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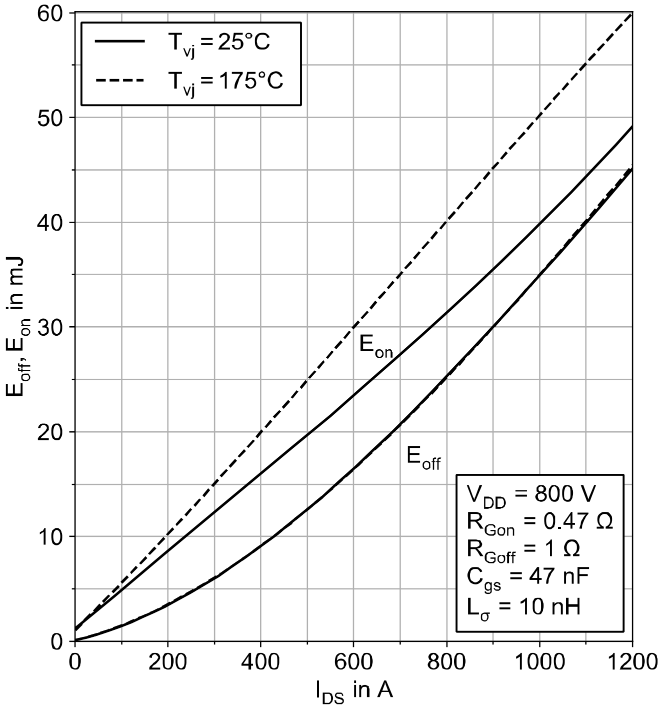

Fig. 8 Typical switching energies per pulse vs. drain current

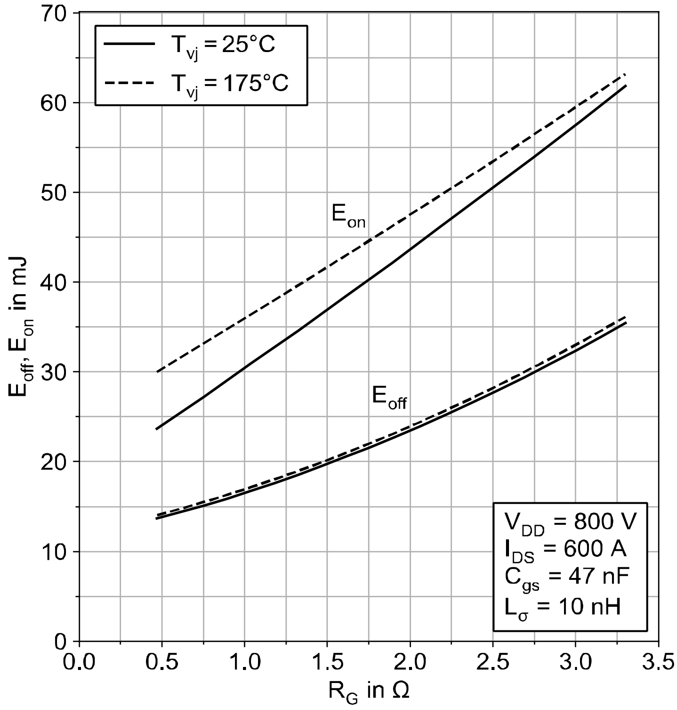

Fig. 9 Typical switching energies per pulse vs. gate resistor

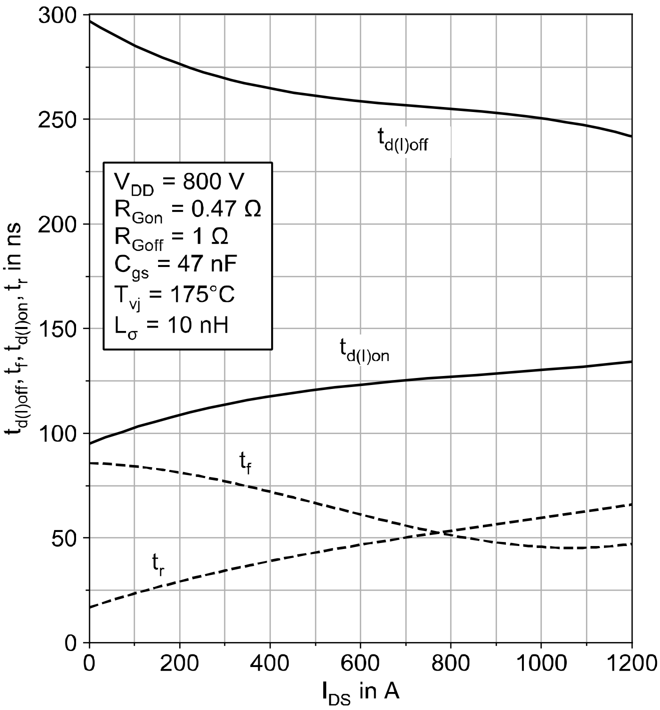

Fig. 10 Typical switching times vs. drain current

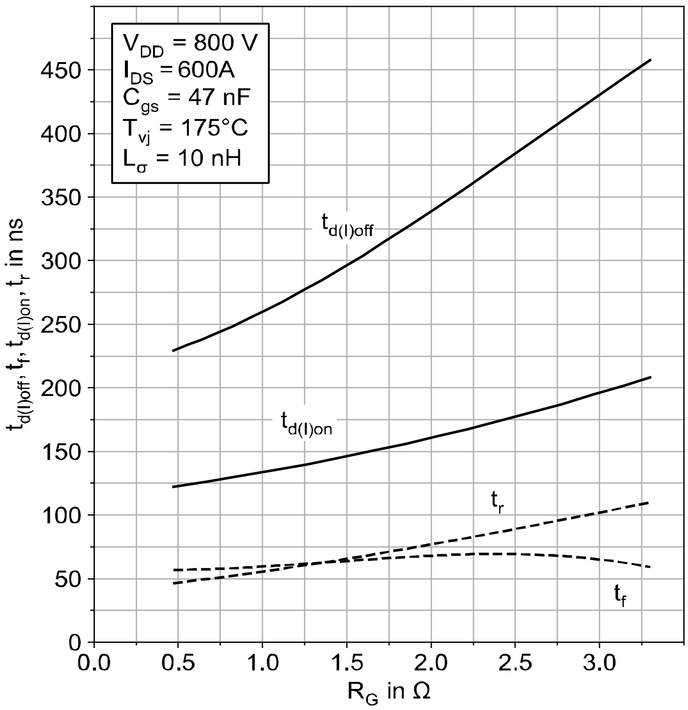

Fig. 11 Typical switching times vs. gate resistor

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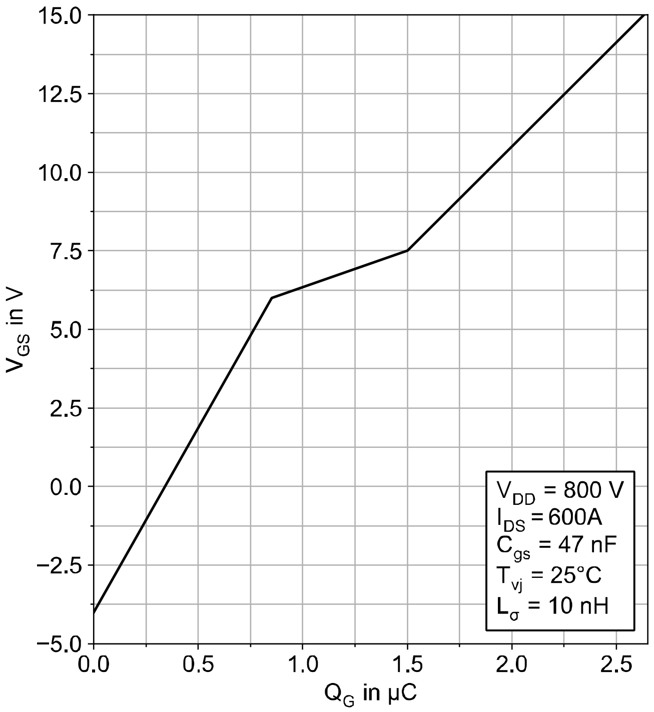

Fig. 12 Typical gate charge characteristics

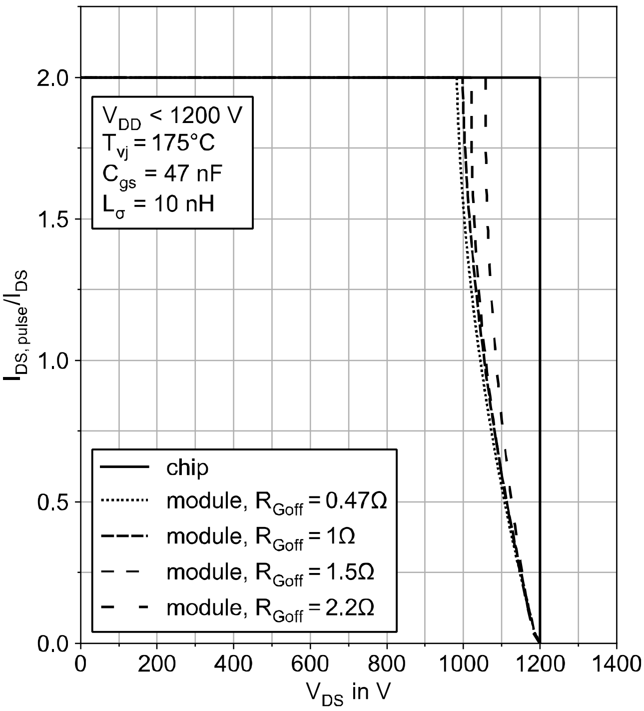

Fig. 13 Turn-off safe operating area (RBSOA)

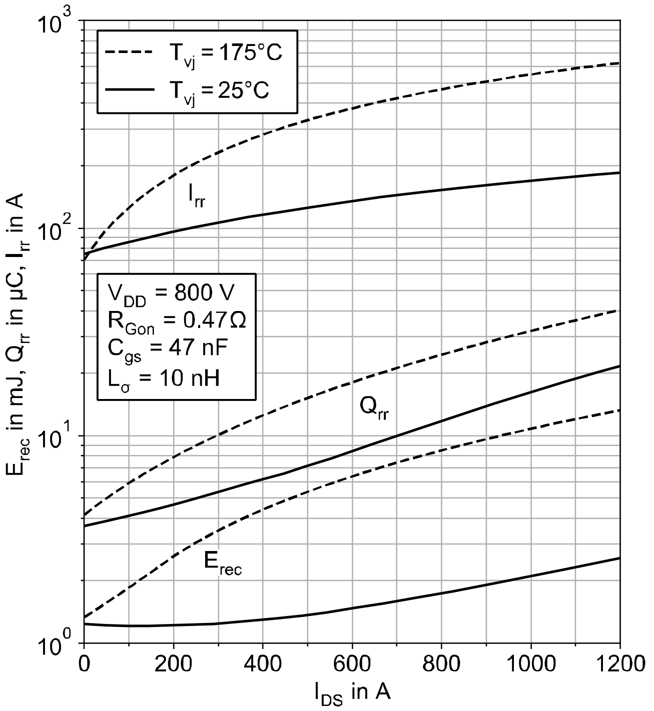

Fig. 14 Typical reverse recovery characteristics vs. forward current

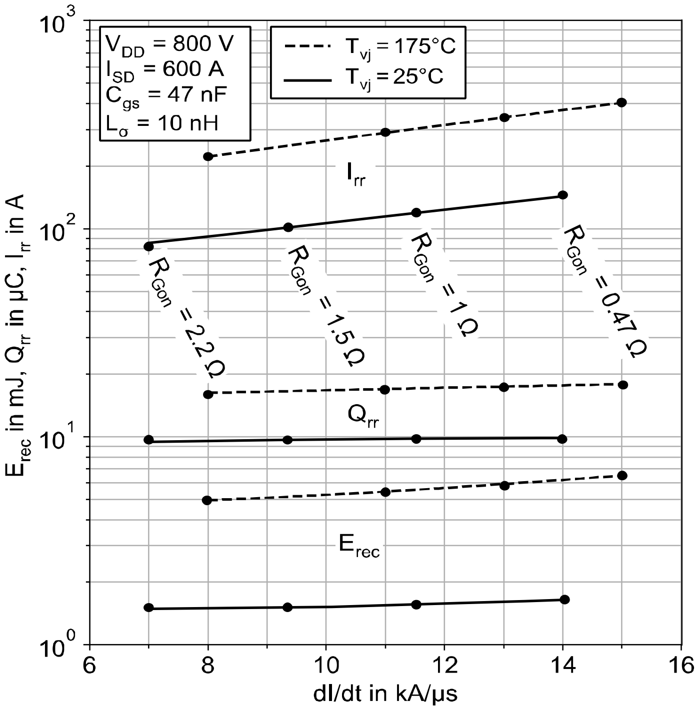

Fig. 15 Typical reverse recovery characteristics vs. di/dt

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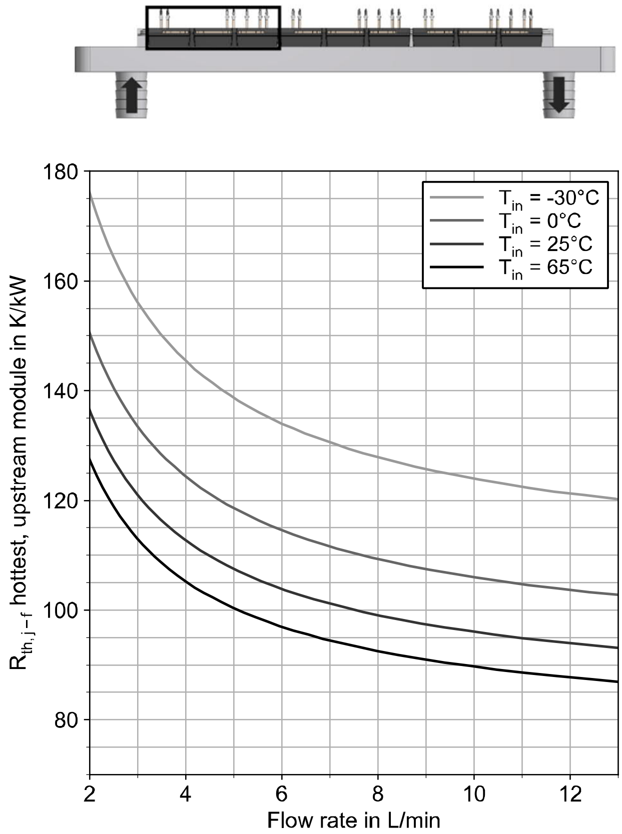

Fig. 16 Thermal resistance vs flow rate, upstream module, hottest chip

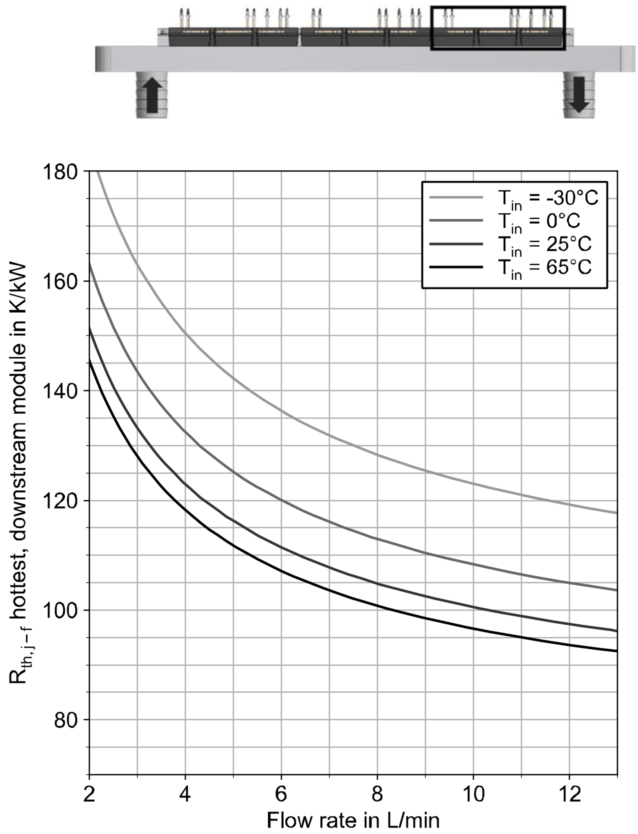

Fig. 17 Thermal resistance vs flow rate, downstream module, hottest chip

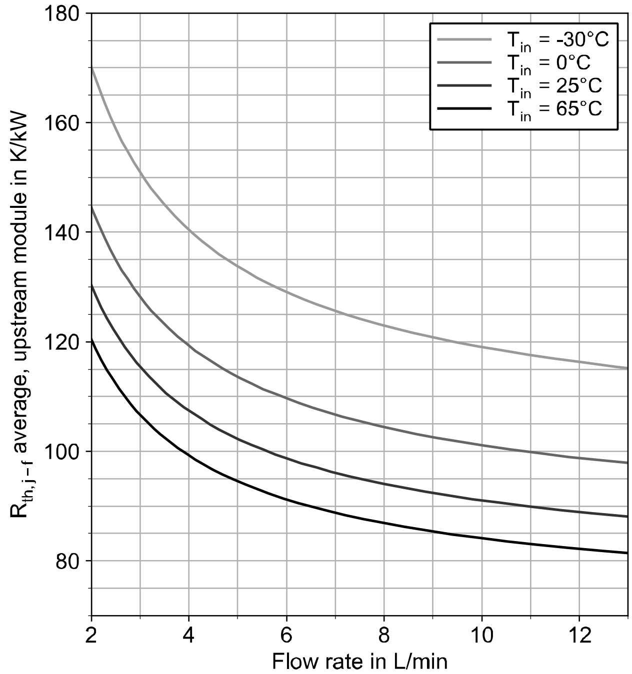

Fig. 18 Thermal resistance vs flow rate, upstream module, average

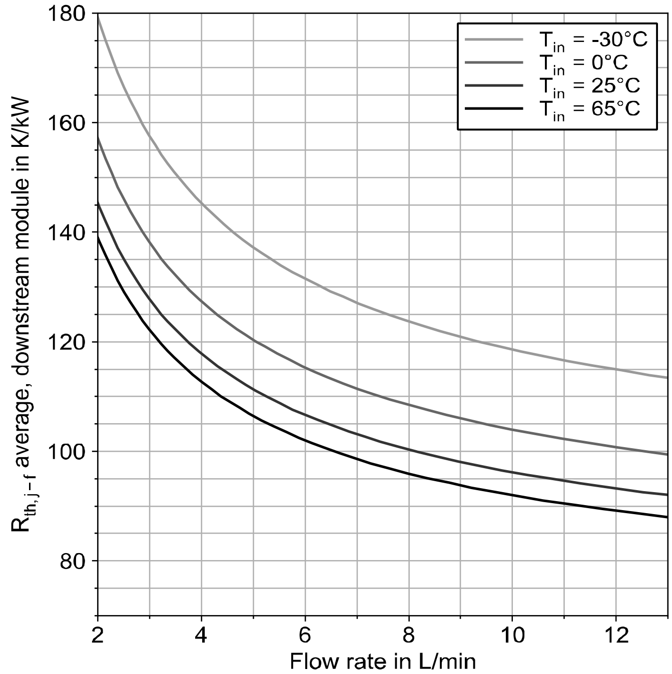

Fig. 19 Thermal resistance vs flow rate, downstream module, average

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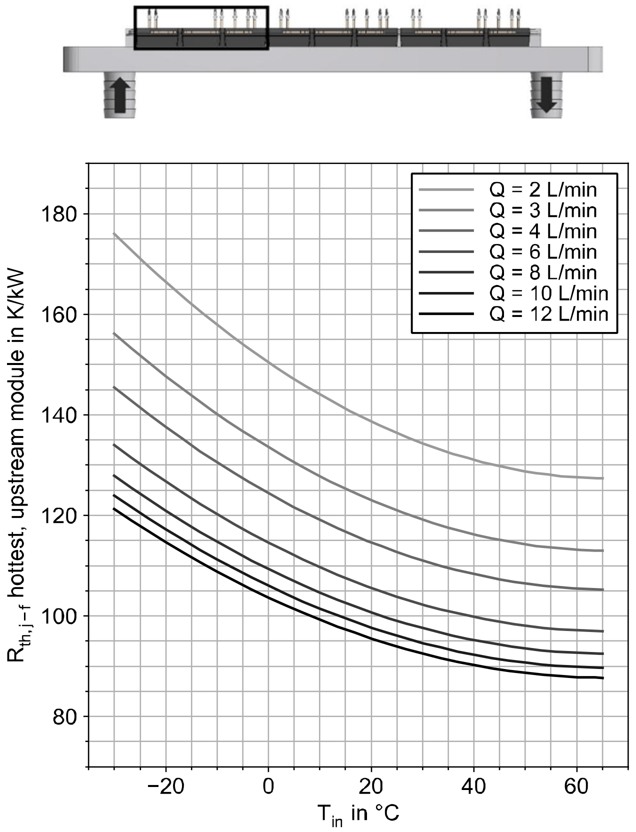

Fig. 20 Thermal resistance vs inlet temperature, upstream module, hottest chip

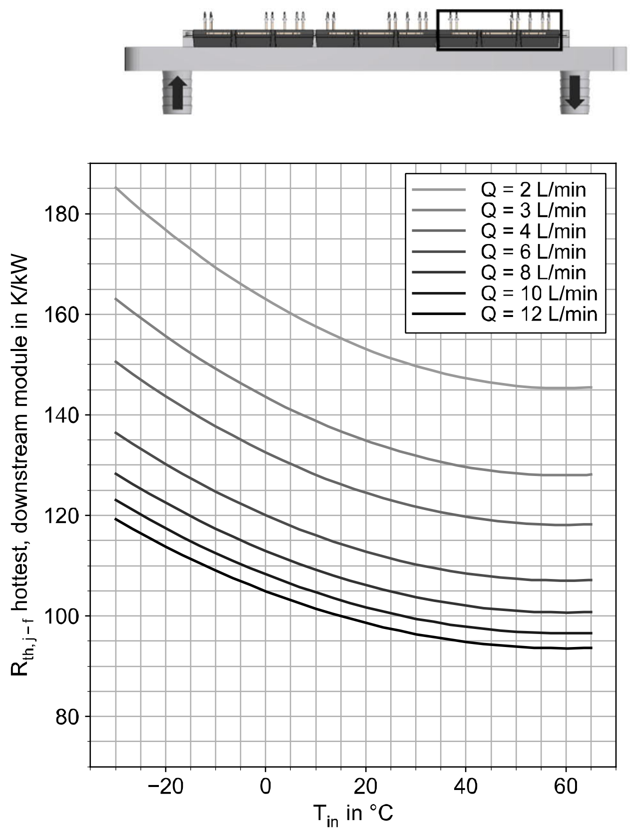

Fig. 21 Thermal resistance vs inlet temperature, downstream module, hottest chip

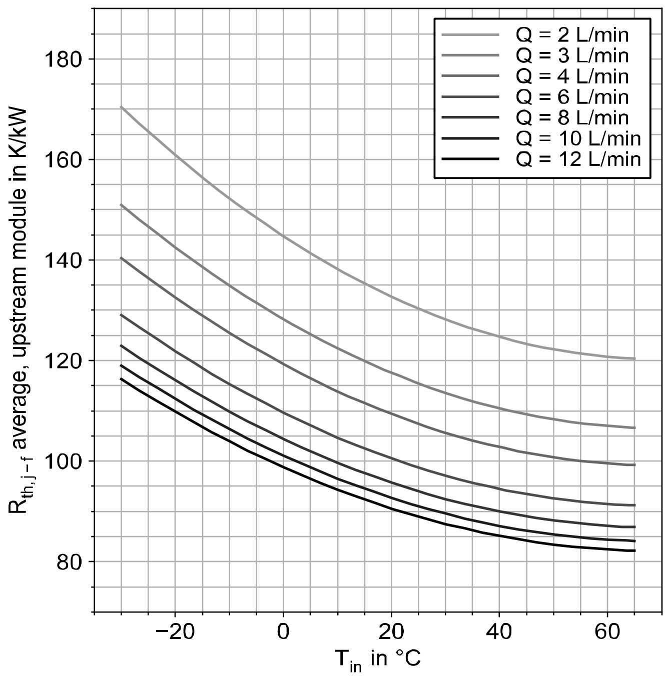

Fig. 22 Thermal resistance vs inlet temperature, upstream module, average

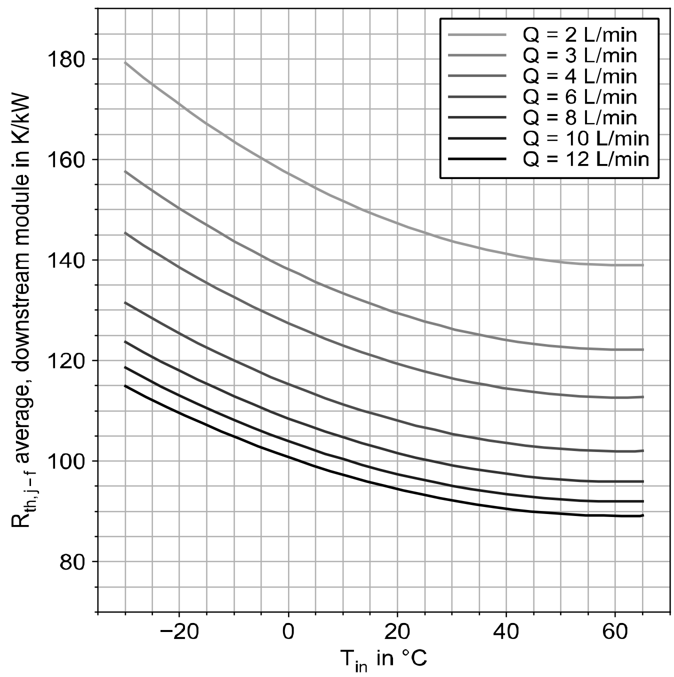

Fig. 23 Thermal resistance vs inlet temperature, downstream module, average

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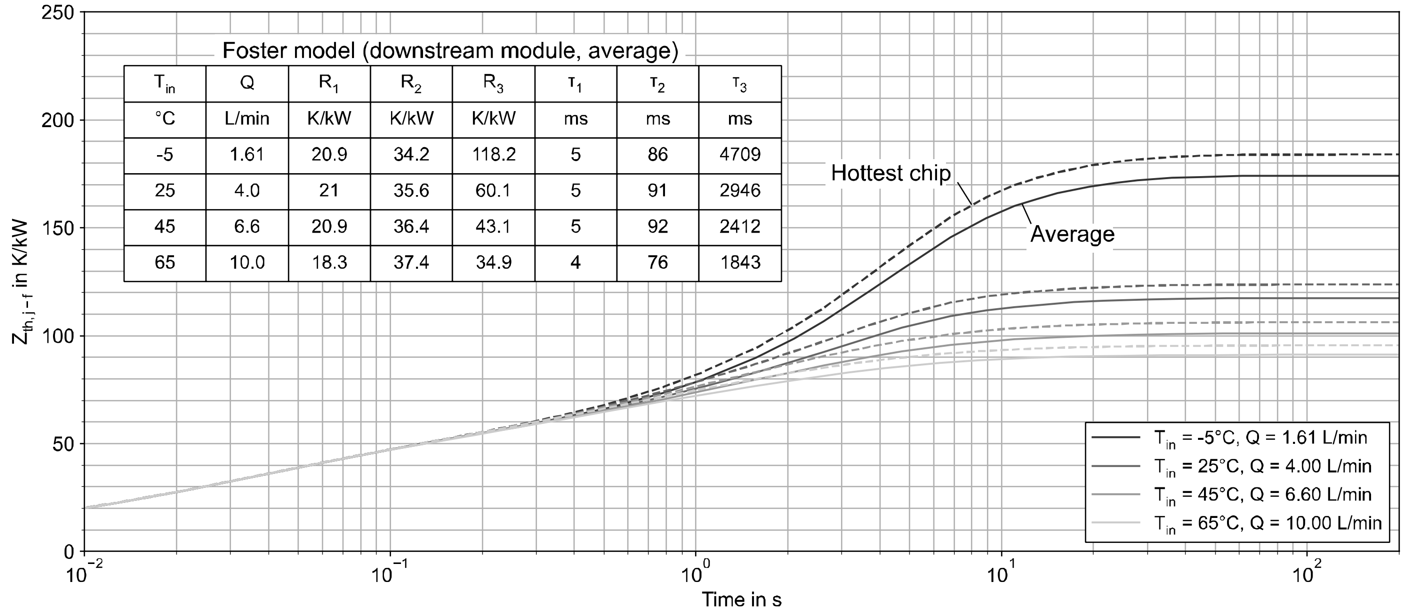
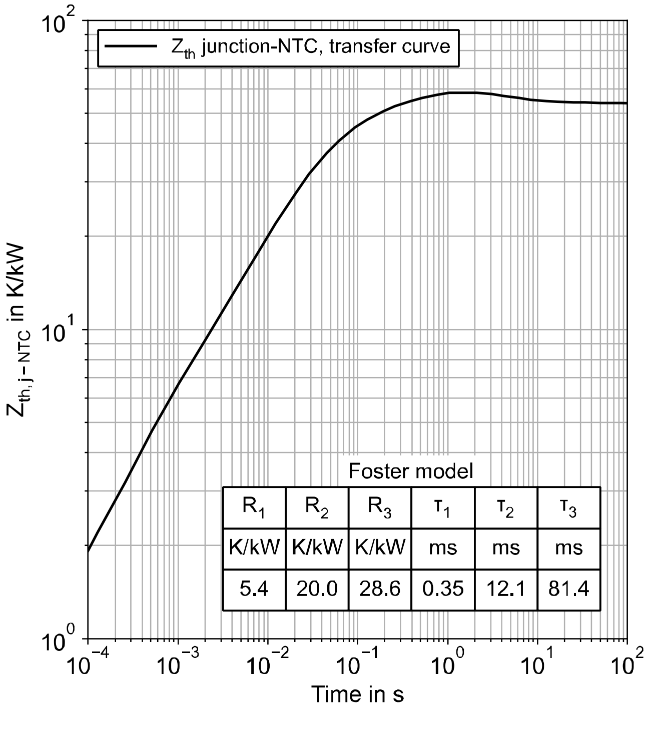


T_{in}	Q	R_1	R_2	R_3	τ_1	τ_2	τ_3
°C	L/min	K/kW	K/kW	K/kW	ms	ms	ms
-5	1.61	20.9	34.2	118.2	5	86	4709
25	4.0	21	35.6	60.1	5	91	2946
45	6.6	20.9	36.4	43.1	5	92	2412
65	10.0	18.3	37.4	34.9	4	76	1843

Fig. 24 Thermal impedance vs time, downstream module



R_1	R_2	R_3	τ_1	τ_2	τ_3
K/kW	K/kW	K/kW	ms	ms	ms
5.4	20.0	28.6	0.35	12.1	81.4

Fig. 25 Thermal impedance vs time, junction to NTC

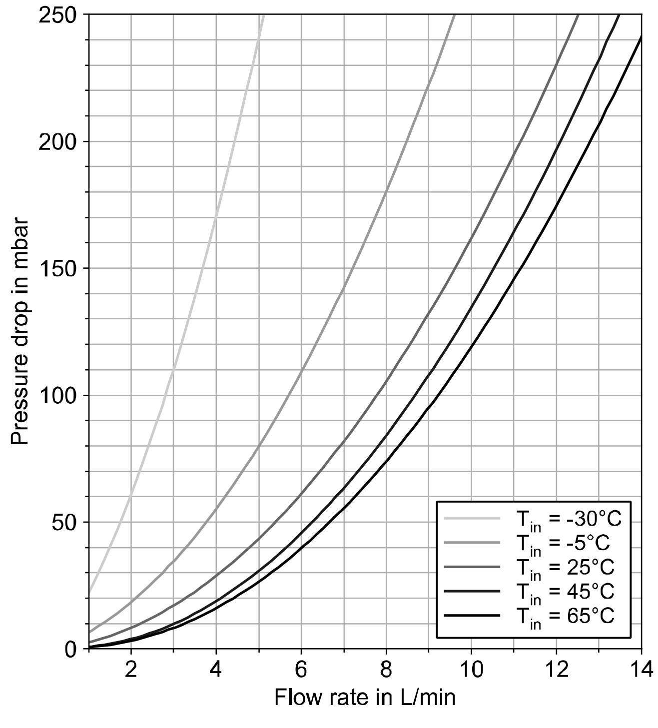


Fig. 26 Pressure drop vs flow rate

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